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[54] PARALLEL-TO-SERIAL-DATA INTERFACE-ADAPTOR

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[58] Field of Search 340/347 DD; 364/200, 364/900

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[57] ABSTRACT

An improved parallel-to-serial-data interface-adaptor

12 Claims, 5 Drawing Figures

that is generally made up of master and slave data processors having master and slave microprocessors, master and slave multibit latches, and separate pairs of read only and random access memories for both the master and slave processors. A data input/output (I/O) bus and an address bus are provided for interconnecting various elements of either the master or slave processors. An interface advantageously interconnects the slave data I/O bus with the master data I/O bus. The master microprocessor advantageously functions to selectively process the master parallel data input when received so that it is compatible with a serial data processor when the selectively processed parallel data input is converted to serial format by a parallel-to-serial-data converter. The master processor further functions by way of the interface to convert a slave parallel data input previously processed by the slave processor to a serial form when the master processor is not busy in processing a parallel data input. The improved master/slave adaptor preferably handles two separate 32-bit parallel data inputs with either input being selectively processed and readily converted by the improved adaptor to a 32-bit serial format that is compatible with a serial data processor.

